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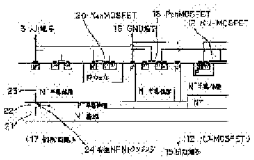
(54) **SEMICONDUCTOR DEVICE**



(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the operation of a parasitic transistor by having a first switch which connects the gate terminal of a power MOSFET with the gate terminal of a first MOSFET.

SOLUTION: This semiconductor device is composed of the Nch MOSFET 20 of a first MOSFET, the pch MOSFET 18 being the second MOSFET to serve as a first switch to control the operation of the Nch MOSFET 20, and a resistor connected in series to this. When the Nch MOSFET 20 is turned on, the area between the base and the emitter of a parasitic NPN transistor 24 short-circuits, in which the n board 21 to become the output of a power MOSFET 12 is a collector, a p type semiconductor layer 22 connected to a GND terminal 16 is a base, and an n semiconductor layer 23 connected to an input terminal 3 is an emitter. Even if the voltage of the input signal source 9 is not more than the voltage of the GND terminal 16, the potential difference between the base and the emitter can be made smaller than the operation voltage (about 0.7V) between the base and the emitter of the parasitic NPN transistor 24, and the operation of the parasitic NPN transistor 24 can be avoided.

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* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] The source of an input signal which generates an input signal, and the power metal-oxide semiconductor field effect transistor which considers a semi-conductor substrate as an output and controls supply of the current to a load, The control circuit which controls actuation of this power metal-oxide semiconductor field effect transistor, and the GND terminal which is a different conductivity type from said semi-conductor substrate, and was prepared in the 1st semi-conductor layer joined to said semi-conductor substrate, Are the same conductivity type as said semi-conductor substrate, and it has the input terminal prepared in the 2nd semi-conductor layer joined to said 1st semi-conductor layer. In the semiconductor device with which the parasitic transistor by which the emitter terminal was connected to said 2nd semi-conductor layer, the collector terminal was connected to said semi-conductor substrate, and the base terminal was connected to said 1st semi-conductor layer into said control circuit exists The 1st MOSFET which a drain terminal is connected to said input terminal, and a source terminal is connected to said GND terminal, and is said semi-conductor substrate and isomorphism channel, The semiconductor device characterized by having the 1st switch which connects the gate terminal of said power metal-oxide semiconductor field effect transistor, and the gate terminal of said 1st MOSFET

when the electrical-potential-difference value in said input terminal is a low level.
[Claim 2] It is the semiconductor device characterized by being the 2nd MOSFET which is the channel of the conductivity type with which said 1st switch differs from said 1st MOSFET in a semiconductor device according to claim 1.
[Claim 3] The semiconductor device characterized by having the current control circuit which controls the current which flows to said control circuit in a semiconductor device according to claim 1 or 2.
[Claim 4] The source of an input signal which generates an input signal, and the power metal-oxide semiconductor field effect transistor which considers a semi-conductor substrate as an output and controls supply of the current to a load, The control circuit which controls actuation of this power metal-oxide semiconductor field effect transistor, and the GND terminal which is a different conductivity type from said semi-conductor substrate, and was prepared in the 1st semi-conductor layer joined to said semi-conductor substrate, Are the same conductivity type as said semi-conductor substrate, and it has the input terminal prepared in the 2nd semi-conductor layer joined to said 1st semi-conductor layer. In the semiconductor device with which the parasitic transistor by which the emitter terminal was connected to said 2nd semi-conductor layer, the collector terminal was connected to said semi-conductor substrate, and the base terminal was connected to said 1st semi-conductor layer into said control circuit exists The semiconductor device characterized by having the 3rd MOSFET by which the drain terminal was connected to said input terminal, the source terminal was connected to said 2nd semi-conductor layer, and the gate terminal was connected to said GND terminal between said 2nd semi-conductor layer and said input terminals.
[Claim 5] The semiconductor device characterized by having the 4th MOSFET by which the drain terminal was connected to the output stage of said control circuit, and the source terminal was connected to said GND terminal in the semiconductor device according to claim 4, and the 2nd switch which connects the gate terminal of said power metal-oxide semiconductor field effect transistor,

and the gate terminal of said 4th MOSFET when the electrical-potential-difference value in said input terminal is a low level.

[Claim 6] It is the semiconductor device characterized by being the 5th MOSFET which is the channel of the conductivity type with which said 2nd switch differs from said semi-conductor substrate in a semiconductor device according to claim 5.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to Power MOSIC about a semiconductor device.

[0002]

[Description of the Prior Art] Drawing 6 is the circuit diagram showing the example of 1 configuration of the conventional semiconductor device.

[0003] The source 9 of an input signal where this conventional example generates an input signal as shown in drawing 6 , The current-limiting resistance 10 which restricts the current which flows to equipment, a power source 13, and

a load 14, The power metal-oxide semiconductor field effect transistor 12 which controls supply of the current to a load 14, and reference diode 25, It consists of diode 26 and a control circuit 17 which controls actuation of power metal-oxide semiconductor field effect transistor 12. In a control circuit 17 Resistance 1 and reference diode 2 which were connected to juxtaposition between the input terminal 3 and the GND terminal 16, Resistance 4 and 5 and the comparator 6 which compares the electrical-potential-difference value in which the partial pressure was carried out by resistance 4 and 5, PchMOSFET7 and NchMOSFET8 as which the output from a comparator 6 is inputted into a gate terminal, One side is connected to the drain terminal of PchMOSFET7 and NchMOSFET8. Parasitism NPN transistor 24 by which the resistance 11 to which another side was connected to the gate terminal of power metal-oxide semiconductor field effect transistor 12 was formed, and the base terminal was connected to the GND terminal 16, the emitter terminal was connected to the input terminal 3, and the collector terminal was connected to the output terminal 15 exists.

[0004] Drawing 7 is the sectional view showing the structure of the semiconductor device shown in drawing 6 .

[0005] This conventional example consists of an N+ substrate 21 used as the output of power metal-oxide semiconductor field effect transistor 12, a P-semi-conductor layer 22 joined on the N+ substrate 21, and an N-semi-conductor layer 23 which is joined on P-semi-conductor layer 22 and has the control circuit 17, as shown in drawing 7 .

[0006] Below, actuation of the semiconductor device constituted as mentioned above is explained.

[0007] Drawing 8 is drawing for explaining actuation of the semiconductor device shown in drawing 6 and drawing 7 , and drawing showing the electrical-potential-difference value in the electrical potential difference of a signal and input terminal 3 with which (a) is outputted from the source 9 of an input signal, drawing in which (b) shows the output voltage of a comparator 6, drawing in which (c)

shows the gate voltage of power metal-oxide semiconductor field effect transistor 12, and (d) are drawings showing the electrical-potential-difference value and current value in an output terminal 15.

[0008] If the electrical potential difference outputted from the source 9 of an input signal rises and the partial pressure electrical-potential-difference value of resistance 4 and 5 exceeds the constant voltage of reference diode 2 (t1), the output of a comparator 6 will serve as a low level.

[0009] Then, PchMOSFET7 will be in an ON state, and NchMOSFET8 will be in an OFF state.

[0010] By this, a charge will be accumulated in the gate of power metal-oxide semiconductor field effect transistor 12, power metal-oxide semiconductor field effect transistor 12 will be in an ON state, and a current flows for a load 14.

[0011] Next, if the electrical potential difference outputted from the source 9 of an input signal falls and the partial pressure electrical-potential-difference value of resistance 4 and 5 becomes below the constant voltage of reference diode 2 (t2), the output of a comparator 6 will become high-level.

[0012] Then, PchMOSFET7 will be in an OFF state, and NchMOSFET8 will be in an ON state.

[0013] The charge accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 discharges by this, and power metal-oxide semiconductor field effect transistor 12 changes to the OFF state.

[0014] And if the electrical potential difference of an output terminal 15 rises and the electrical potential difference of an output terminal 15 exceeds the constant-voltage value of reference diode 25 by the reactance component of a load 14, it will pass along reference diode 25, diode 26, and resistance 11, and a current will flow to an input terminal 3 from the GND terminal 16 from NchMOSFET8, or the drain of PchMOSFET7.

[0015] Thereby, bias of the gate voltage of power metal-oxide semiconductor field effect transistor 12 is carried out succeedingly, and the so-called dynamic clamp actuation to which a current flows to power metal-oxide semiconductor

field effect transistor 12 by this bias is performed.

[0016]

[Problem(s) to be Solved by the Invention] However, in the conventional semiconductor device which was mentioned above, when the electrical potential difference of an input terminal 3 becomes lower than the electrical potential difference of the GND terminal 16, parasitism NPN transistor 24 operates and there is a trouble that a current will flow from an output terminal 15 to an input terminal 3, and equipment will be damaged.

[0017] Namely, as shown in drawing 7 , it sets for the above-mentioned conventional example. Since the N+ substrate 21 is the structure where the base and N-semi-conductor layer 23 serve as [parasitism NPN transistor 24 / a collector and P-semi-conductor layer 22] an emitter, where an electrical potential difference is impressed to an output terminal 15 If the electrical potential difference in an input terminal 3 becomes lower than the electrical potential difference in the GND terminal 16 and a current flows [the difference] from the GND terminal 16 to an input terminal 3 exceeding the electrical potential difference between base emitters, parasitism NPN transistor 24 will operate.

[0018] When the high electrical potential difference (for example, 70V) is especially impressed to the output terminal 15 like [at the time of dynamic clamp actuation], it becomes second breakdown peculiar to a bipolar transistor, and becomes easy to generate breakage of equipment.

[0019] Then, the equipment which prevents breakage of a semiconductor device to JP,5-58583,A is indicated.

[0020] Drawing 9 is the block diagram showing the outline of the equipment indicated by JP,5-58583,A.

[0021] This equipment makes it flow through MOSFET31 by the secondary breakdown, when high MOSFET31 of threshold voltage VT is connected between the input terminal 3 and the GND terminal 16, static electricity is impressed to an input terminal 3 and the electrical potential difference between an input terminal 3 and the GND terminal 16 exceeds threshold voltage VT

(about [This example 20-25] V), as shown in drawing 9 .

[0022] However, since the trouble in the semiconductor device shown in drawing 6 is breakage of the equipment generated when parasitism NPN transistor 24 operates when the electrical potential difference of an input terminal 3 is lower than the electrical potential difference of the GND terminal 16, the well-known example shown in drawing 9 does not make semantics.

[0023] Moreover, there is Supply Terminal Protection of "Reverse-Voltage Protection Methods for CMOSCircuits" (IEEE JOURNAL Vol24, Feb.1989) as other well-known examples.

[0024] Drawing 10 is the block diagram showing the outline of the equipment indicated by "Reverse-Voltage Protection Methods for CMOS Circuits" (IEEE JOURNAL Vol24, Feb.1989), and drawing 11 is the sectional view showing the structure of the equipment shown in drawing 10 .

[0025] This equipment is what connected PchMOSFET34 between VDD32 and the N substrate 33 as shown in drawing 10 and drawing 11 , and it prevents a short-circuit current flowing through the parasitism diode 35 at the time of VDD<VSS.

[0026] However, in the semiconductor device shown in drawing 6 , since the current-limiting resistance 10 is inserted, even if it inputs VDD32 and replaces VSS with GND, the cure which prevents a short-circuit current is unnecessary. Moreover, if power metal-oxide semiconductor field effect transistor is carried in the equipment shown in drawing 10 and drawing 11 , since it will become the power metal-oxide semiconductor field effect transistor of a high proof-pressure horizontal type to it, on resistance becomes large and (they are about 1.5 times for example, by 70V pressure-proofing) is unsuitable.

[0027] This invention is made in view of the trouble which a Prior art which was mentioned above has, and aims at offering the semiconductor device which can prevent breakage of the equipment generated when a parasitic transistor operates.

[0028]

[Means for Solving the Problem] The source of an input signal where this invention generates an input signal in order to attain the above-mentioned purpose, The power metal-oxide semiconductor field effect transistor which considers a semi-conductor substrate as an output and controls supply of the current to a load, The control circuit which controls actuation of this power metal-oxide semiconductor field effect transistor, and the GND terminal which is a different conductivity type from said semi-conductor substrate, and was prepared in the 1st semi-conductor layer joined to said semi-conductor substrate, Are the same conductivity type as said semi-conductor substrate, and it has the input terminal prepared in the 2nd semi-conductor layer joined to said 1st semi-conductor layer. In the semiconductor device with which the parasitic transistor by which the emitter terminal was connected to said 2nd semi-conductor layer, the collector terminal was connected to said semi-conductor substrate, and the base terminal was connected to said 1st semi-conductor layer into said control circuit exists The 1st MOSFET which a drain terminal is connected to said input terminal, and a source terminal is connected to said GND terminal, and is said semi-conductor substrate and isomorphism channel, When the electrical-potential-difference value in said input terminal is a low level, it is characterized by having the 1st switch which connects the gate terminal of said power metal-oxide semiconductor field effect transistor, and the gate terminal of said 1st MOSFET.

[0029] Moreover, said 1st switch is characterized by being the 2nd MOSFET which is the channel of a different conductivity type from said 1st MOSFET.

[0030] Moreover, it is characterized by having the current control circuit which controls the current which flows to said control circuit.

[0031] Moreover, the source of an input signal which generates an input signal and power metal-oxide semiconductor field effect transistor which considers a semi-conductor substrate as an output and controls supply of the current to a load, The control circuit which controls actuation of this power metal-oxide semiconductor field effect transistor, and the GND terminal which is a different

conductivity type from said semi-conductor substrate, and was prepared in the 1st semi-conductor layer joined to said semi-conductor substrate, Are the same conductivity type as said semi-conductor substrate, and it has the input terminal prepared in the 2nd semi-conductor layer joined to said 1st semi-conductor layer. In the semiconductor device with which the parasitic transistor by which the emitter terminal was connected to said 2nd semi-conductor layer, the collector terminal was connected to said semi-conductor substrate, and the base terminal was connected to said 1st semi-conductor layer into said control circuit exists It is characterized by having the 3rd MOSFET by which the drain terminal was connected to said input terminal, the source terminal was connected to said 2nd semi-conductor layer, and the gate terminal was connected to said GND terminal between said 2nd semi-conductor layer and said input terminals.

[0032] Moreover, it is characterized by having the 4th MOSFET by which the drain terminal was connected to the output stage of said control circuit, and the source terminal was connected to said GND terminal, and the 2nd switch which connects the gate terminal of said power metal-oxide semiconductor field effect transistor, and the gate terminal of said 4th MOSFET when the electrical-potential-difference value in said input terminal is a low level.

[0033] Moreover, said 2nd switch is characterized by being the 5th MOSFET which is the channel of a different conductivity type from said semi-conductor substrate.

[0034] (Operation) In this invention constituted as mentioned above, since the 1st MOSFET will be in an ON state by actuation of the 1st switch and between the base emitters of a parasitic transistor connects too hastily by that cause in case the charge accumulated in power metal-oxide semiconductor field effect transistor discharges, a parasitic transistor does not operate.

[0035] Moreover, since the 3rd MOSFET will be in an OFF state when the source electrical potential difference of the 3rd MOSFET falls and a difference with gate voltage becomes threshold voltage, the emitter electrical potential difference of a parasitic transistor does not become lower than a base electrical potential

difference, and a parasitic transistor does not operate.

[0036]

[Embodiment of the Invention] Below, the gestalt of operation of this invention is explained with reference to a drawing.

[0037] (Gestalt of the 1st operation) Drawing 1 is the circuit diagram showing the gestalt of operation of the 1st of the semiconductor device of this invention, and drawing 2 is the sectional view showing the structure of the semiconductor device shown in drawing 1 .

[0038] The source 9 of an input signal where this gestalt generates an input signal as shown in drawing 1 , The current-limiting resistance 10 which restricts the current which flows to equipment, a power source 13, and a load 14, The power metal-oxide semiconductor field effect transistor 12 which controls supply of the current to a load 14, and reference diode 25, Diode 26 and the control circuit 17 which controls actuation of power metal-oxide semiconductor field effect transistor 12, NchMOSFET20 which is the 1st MOSFET connected to juxtaposition between the input terminal 3 of a control circuit 17, and the GND terminal 16, PchMOSFET18 which is the 2nd MOSFET used as the 1st switch which controls actuation of NchMOSFET20, It consists of resistance 19 connected to PchMOSFET18 and a serial. In a control circuit 17 Resistance 1 and reference diode 2 which were connected to juxtaposition between the input terminal 3 and the GND terminal 16, Resistance 4 and 5 and the comparator 6 which compares the electrical-potential-difference value in which the partial pressure was carried out by resistance 4 and 5, PchMOSFET7 and NchMOSFET8 as which the output from a comparator 6 is inputted into a gate terminal, One side is connected to the drain terminal of PchMOSFET7 and NchMOSFET8. Parasitism NPN transistor 24 by which the resistance 11 to which another side was connected to the gate terminal of power metal-oxide semiconductor field effect transistor 12 was formed, and the base terminal was connected to the GND terminal 16, the emitter terminal was connected to the input terminal 3, and the collector terminal was connected to the output terminal

15 exists. In addition, in NchMOSFET20, a gate terminal is connected to the GND terminal 16 through resistance 19, a source terminal is connected to the GND terminal 16, the drain terminal is connected to the input terminal 3, in PchMOSFET18, a gate terminal is connected to an input terminal 3, a drain terminal is connected to the gate terminal of NchMOSFET20, and the source terminal is connected to the gate terminal of power metal-oxide semiconductor field effect transistor 12.

[0039] In the semiconductor device constituted as mentioned above, the electrical-potential-difference value by which reference voltage was generated, was inputted by resistance 1 and reference diode 2 from this reference voltage and input terminal 3, and the partial pressure was carried out by resistance 4 and 5 with them is compared in the comparator 6.

[0040] Moreover, the N+ substrate 21 which serves as an output of power metal-oxide semiconductor field effect transistor 12 as this gestalt is shown in drawing 2 , P-semi-conductor layer 22 which is the 1st semi-conductor layer joined on the N+ substrate 21, It is joined on P-semi-conductor layer 22, and consists of N-semi-conductor layers 23 which are the 2nd semi-conductor layer which has the control circuit 17, and on the N+ substrate 21, an input terminal 3 is formed on N-semi-conductor layer 23, and the GND terminal 16 is formed for the output terminal 15 on P-semi-conductor layer 22, respectively.

[0041] Below, actuation of the semiconductor device constituted as mentioned above is explained.

[0042] If the electrical potential difference outputted from the source 9 of an input signal rises and the partial pressure electrical-potential-difference value of resistance 4 and 5 exceeds the constant voltage of reference diode 2, the output of a comparator 6 will serve as a low level.

[0043] Then, PchMOSFET7 will be in an ON state, and NchMOSFET8 will be in an OFF state.

[0044] By this, a charge will be accumulated in the gate of power metal-oxide semiconductor field effect transistor 12, power metal-oxide semiconductor field

effect transistor 12 will be in an ON state, and a current flows for a load 14, an output terminal 15, and the GND terminal 16 from a power source 13.

[0045] Next, if the electrical potential difference outputted from the source 9 of an input signal falls and the partial pressure electrical-potential-difference value of resistance 4 and 5 becomes below the constant voltage of reference diode 2, the output of a comparator 6 will become high-level.

[0046] Then, PchMOSFET7 will be in an OFF state, and NchMOSFET8 will be in an ON state.

[0047] Although the charge accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 begins to discharge by this, in this case, PchMOSFET18 will be in an ON state, thereby, an electrical potential difference will be impressed to resistance 19, and NchMOSFET20 will be in an ON state.

[0048] By this, as shown in drawing 2 , the N+ substrate 21 used as the output of power metal-oxide semiconductor field effect transistor 12 is used as a collector. Will use as the base P-semi-conductor layer 22 connected to the GND terminal 16, and between the base emitters of parasitism NPN transistor 24 used as an emitter will short-circuit N-semi-conductor layer 23 connected to the input terminal 3. Since the electrical potential difference in the source 9 of an input signal can make the electrical-potential-difference difference between base emitters smaller than the operating voltage between base emitters of parasitism NPN transistor 24 (about 0.7 V) also in a case of below [the electrical potential difference in the GND terminal 16], Actuation of parasitism NPN transistor 24 is avoided.

[0049] Next, if the gate voltage of power metal-oxide semiconductor field effect transistor 12 falls, the electrical potential difference in an output terminal 15 will rise, it will pass along between reference diode 25, diode 26, resistance 11, and the drain source of PchMOSFET7, and a current will flow for an input terminal 3 or PchMOSFET18, resistance 19, and the GND terminal 16.

[0050] PchMOSFET18 will be in an ON state and NchMOSFET20 will be in an ON state, and when the electrical potential difference in an output terminal 15 is

high, it can prevent parasitism NPN transistor 24 operating, until the energy accumulated in the reactance of a load 14 is emitted and the electrical potential difference in an output terminal 15 falls, since bias of the gate of power metal-oxide semiconductor field effect transistor 12 is carried out by this current.

[0051] (Gestalt of the 2nd operation) Drawing 3 is the circuit diagram showing the gestalt of operation of the 2nd of the semiconductor device of this invention.

[0052] The source 9 of an input signal where this gestalt generates an input signal as shown in drawing 3 , A power source 13, a load 14, and the power metal-oxide semiconductor field effect transistor 12 that controls supply of the current to a load 14, It consists of PchMOSFET(s)27 which are the 3rd MOSFET connected between the control circuit 17 which controls actuation of power metal-oxide semiconductor field effect transistor 12, and the source 9 of an input signal and a control circuit 17. Resistance 1 and reference diode 2 which were connected to juxtaposition between the source terminal of PchMOSFET27, and the GND terminal 16 in the control circuit 17, Resistance 4 and 5 and the comparator 6 which compares the electrical-potential-difference value in which the partial pressure was carried out by resistance 4 and 5, PchMOSFET7 and NchMOSFET8 as which the output from a comparator 6 is inputted into a gate terminal, One side is connected to the drain terminal of PchMOSFET7 and NchMOSFET8. The resistance 11 to which another side was connected to the gate terminal of power metal-oxide semiconductor field effect transistor 12 is formed. Moreover, parasitism NPN transistor 24 by which the base terminal was connected to the GND terminal 16, the emitter terminal was connected to the source terminal of PchMOSFET27, and the collector terminal was connected to the output terminal 15 exists. In addition, in PchMOSFET27, a gate terminal is connected to the GND terminal 16, a source terminal is connected to a control circuit 17, and the drain terminal is connected to the input terminal 3.

[0053] Below, actuation of the semiconductor device constituted as mentioned above is explained.

[0054] If PchMOSFET27 will be in an ON state and the electrical potential

difference in the source 9 of an input signal will rise further, if the electrical potential difference in the source 9 of an input signal rises and the sum of the diode voltage between the drain sources of PchMOSFET27 (about 0.7 V) and threshold voltage (about 1 V) is exceeded, and it becomes high-level, a charge will be accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 by actuation of a control circuit 17, and power metal-oxide semiconductor field effect transistor 12 will be in an ON state.

[0055] Next, if the electrical potential difference of the source 9 of an input signal falls and it becomes below an electrical potential difference in the GND terminal 16, the charge accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 will flow into an input terminal 3 out of PchMOSFET27 to which bias of the gate is carried out through resistance 11 and the diode between the drain sources of PchMOSFET7.

[0056] Drawing 4 is drawing for explaining actuation of the semiconductor device shown in drawing 3 , and drawing showing an electrical-potential-difference value [in / in (a) / an input terminal 3], drawing in which (b) shows the source electrical potential difference of PchMOSFET27, and (c) are drawings showing the electrical-potential-difference value and current value in an output terminal 15.

[0057] When the source electrical potential difference of PchMOSFET27 reaches the low level of a control circuit 17, and the high-level judgment electrical potential difference VIHL, NchMOSFET8 will be in an ON state, the source electrical potential difference of PchMOSFET27 turns into about 0 electrical potential differences, and a control circuit 17 stops operating thereby.

[0058] Therefore, if the charge with which NchMOSFET8 was accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 in the unstable condition of calling it an OFF state discharges and discharge is completed, power metal-oxide semiconductor field effect transistor 12 will be in an OFF state.

[0059] Although the source electrical potential difference of PchMOSFET27 falls gradually at this time, since PchMOSFET27 will be in an OFF state with threshold voltage (about 1 V), it does not become below an electrical potential

difference in the GND terminal 16. Therefore, parasitism NPN transistor 24 does not operate.

[0060] If a current flows to PchMOSFET27 until the charge accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 when the electrical potential difference in the source 9 of an input signal turned into below the electrical potential difference in the GND terminal 16 in this gestalt discharges and discharge is completed as explained above, and discharge is completed, since it will become actuation that a current does not flow, a parasitic transistor does not operate.

[0061] (Gestalt of the 3rd operation) Drawing 5 is the circuit diagram showing the gestalt of operation of the 3rd of the semiconductor device of this invention.

[0062] The source 9 of an input signal where this gestalt generates an input signal as shown in drawing 5 , A power source 13, a load 14, and the power metal-oxide semiconductor field effect transistor 12 that controls supply of the current to a load 14, The control circuit 17 which controls actuation of power metal-oxide semiconductor field effect transistor 12, and NchMOSFET30 which is the 4th MOSFET connected to the output stage of a control circuit 17, PchMOSFET28 which is the 5th MOSFET used as the 2nd switch which controls actuation of NchMOSFET30, It consists of resistance 29 connected to PchMOSFET28 and a serial, and PchMOSFET27 connected between the source 9 of an input signal, and the control circuit 17. In a control circuit 17 Resistance 1 and reference diode 2 which were connected to juxtaposition between the source terminal of PchMOSFET27, and the GND terminal 16, Resistance 4 and 5 and the comparator 6 which compares the electrical-potential-difference value in which the partial pressure was carried out by resistance 4 and 5, PchMOSFET7 and NchMOSFET8 as which the output from a comparator 6 is inputted into a gate terminal, One side is connected to the drain terminal of PchMOSFET7 and NchMOSFET8. The resistance 11 to which another side was connected to the gate terminal of power metal-oxide semiconductor field effect transistor 12 is formed. Moreover, parasitism NPN transistor 24 by which the base terminal was

connected to the GND terminal 16, the emitter terminal was connected to the source terminal of PchMOSFET27, and the collector terminal was connected to the output terminal 15 exists. In addition, in NchMOSFET30, a gate terminal is connected to the GND terminal 16 through resistance 29, a source terminal is connected to the GND terminal 16, the drain terminal is connected to the drain terminal of PchMOSFET7 and NchMOSFET8, in PchMOSFET28, a gate terminal is connected to an input terminal 3, a drain terminal is connected to the gate terminal of NchMOSFET30, and the source terminal is connected to the gate terminal of power metal-oxide semiconductor field effect transistor 12.

[0063] Below, actuation of the semiconductor device constituted as mentioned above is explained.

[0064] If the electrical potential difference in the source 9 of an input signal turns into below the electrical potential difference in the GND terminal 16, PchMOSFET28 will be in an ON state and, thereby, NchMOSFET30 will be in an ON state.

[0065] And the charge accumulated in the gate of power metal-oxide semiconductor field effect transistor 12 discharges through resistance 11 and NchMOSFET30.

[0066] Therefore, since the electrical potential difference between the gate sources of PchMOSFET27 is set to about 0 while a control circuit 17 does not serve as unstable actuation but being turned off, a current will not flow to PchMOSFET27.

[0067] Therefore, even when the signal outputted from the source 9 of an input signal is based on other semiconductor devices with little drive capacity etc., the high-speed turn-off time can be secured.

[0068] In addition, in the gestalt of operation mentioned above, although the circuit where a parasitism NPN transistor exists using Nch power metal-oxide semiconductor field effect transistor was explained, when a parasitism PNP transistor exists using PchMOSFET, the same effectiveness can be raised by setting NchMOSFET and PchMOSFET28 to NchMOSFET and setting

[PchMOSFET18 / NchMOSFET and NchMOSFET20] NchMOSFET30 to PchMOSFET for PchMOSFET and PchMOSFET27.

[0069]

[Effect of the Invention] Since this invention is constituted as explained above, it does so effectiveness which is indicated below.

[0070] In case the charge accumulated in claims 1-3 in the thing of a publication at power metal-oxide semiconductor field effect transistor discharges, the 1st MOSFET can be in an ON state by actuation of the 1st switch, it can write by that cause as the configuration which between the base emitters of a parasitic transistor short-circuits, a parasitic transistor cannot operate, and breakage of a semiconductor device can be prevented.

[0071] In a thing given in claims 4 and 5, when the source electrical potential difference of the 3rd MOSFET falls and a difference with gate voltage becomes threshold voltage, it writes as the configuration in which the 3rd MOSFET will be in an OFF state, the emitter electrical potential difference of a parasitic transistor does not become lower than a base electrical potential difference, and a parasitic transistor does not operate. Thereby, breakage of the semiconductor device generated by actuation of a parasitic transistor can be prevented.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the gestalt of operation of the 1st of the semiconductor device of this invention.

[Drawing 2] It is the sectional view showing the structure of the semiconductor device shown in drawing 1 .

[Drawing 3] It is the circuit diagram showing the gestalt of operation of the 2nd of the semiconductor device of this invention.

[Drawing 4] It is drawing for explaining actuation of the semiconductor device shown in drawing 3 , and drawing showing an electrical-potential-difference value [in / in (a) / an input terminal], drawing in which (b) shows the source electrical potential difference of PchMOSFET, and (c) are drawings showing the electrical-potential-difference value and current value in an output terminal.

[Drawing 5] It is the circuit diagram showing the gestalt of operation of the 3rd of the semiconductor device of this invention.

[Drawing 6] It is the circuit diagram showing the example of 1 configuration of the conventional semiconductor device.

[Drawing 7] It is the sectional view showing the structure of the semiconductor device shown in drawing 6 .

[Drawing 8] It is drawing for explaining actuation of the semiconductor device shown in drawing 6 and drawing 7 , and drawing showing the electrical-potential-difference value in the electrical potential difference of a signal and input terminal 3 with which (a) is outputted from the source 9 of an input signal, drawing in which (b) shows the output voltage of a comparator 6, drawing in which (c) shows the gate voltage of power metal-oxide semiconductor field effect transistor 12, and (d) are drawings showing the electrical-potential-difference value and current value in an output terminal 15.

[Drawing 9] It is the block diagram showing the outline of the equipment indicated by JP,5-58583,A.

[Drawing 10] It is the block diagram showing the outline of the equipment indicated by "Reverse-Voltage Protection Methods for CMOS Circuits" (IEEE JOURNALVol24, Feb.1989).

[Drawing 11] It is the sectional view showing the structure of the equipment shown in drawing 10 .

[Description of Notations]

1, 4, 5, 11, 19, 29 Resistance

2 25 Reference diode

3 Input Terminal

6 Comparator

7,18,27,28,34 PchMOSFET

8,20,30 NchMOSFET

9 Source of Input Signal

10 Current-Limiting Resistance

12 Power Metal-oxide Semiconductor Field Effect Transistor

13 Power Source

14 Load

15 Output Terminal

16 GND Terminal

17 Control Circuit

21 N+ Substrate

22 P-Semi-conductor Layer

23 N-Semi-conductor Layer

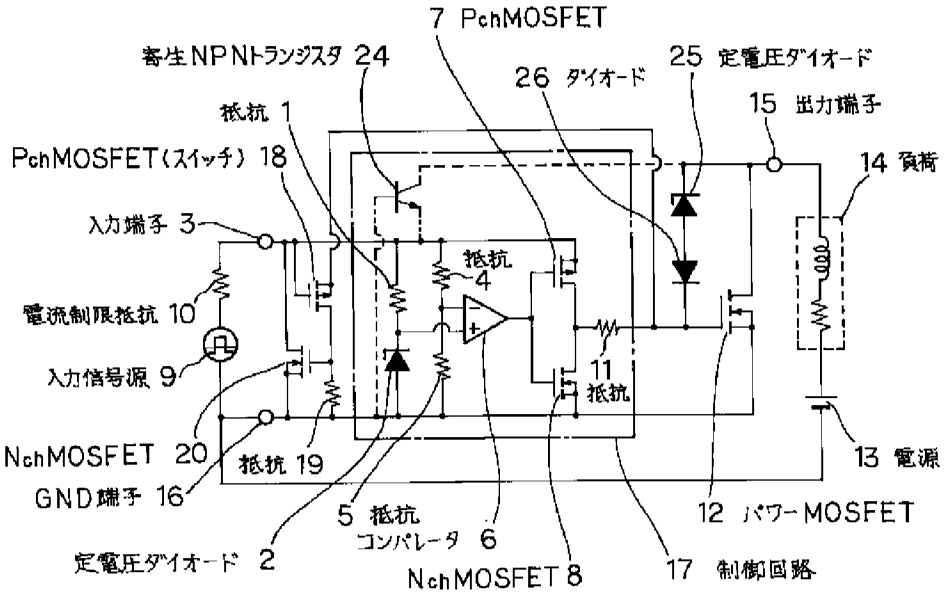
24 Parasitism NPN Transistor

26 Diode

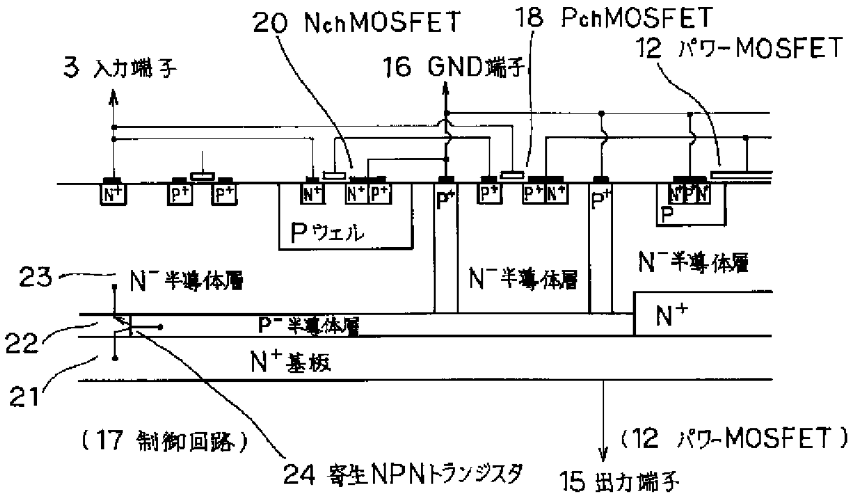
[Translation done.]

DRAWINGS

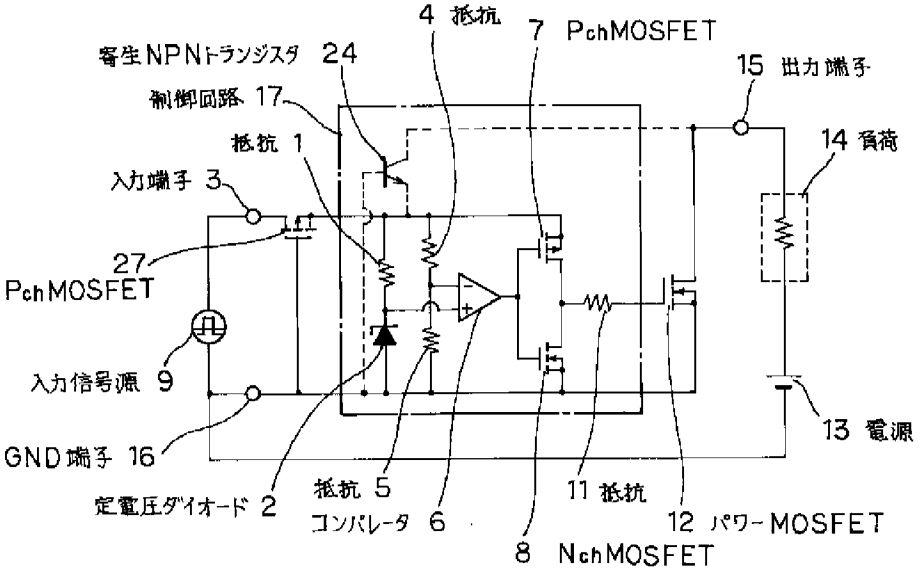
[Drawing 1]



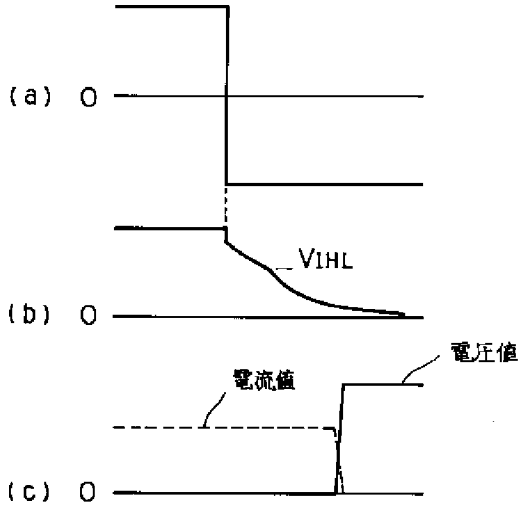
[Drawing 2]



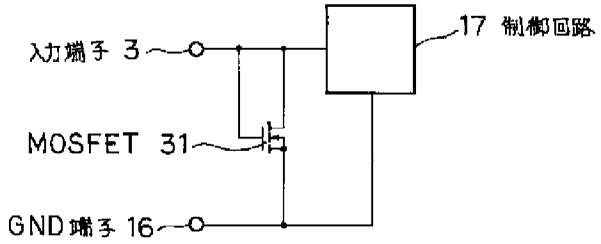
[Drawing 3]



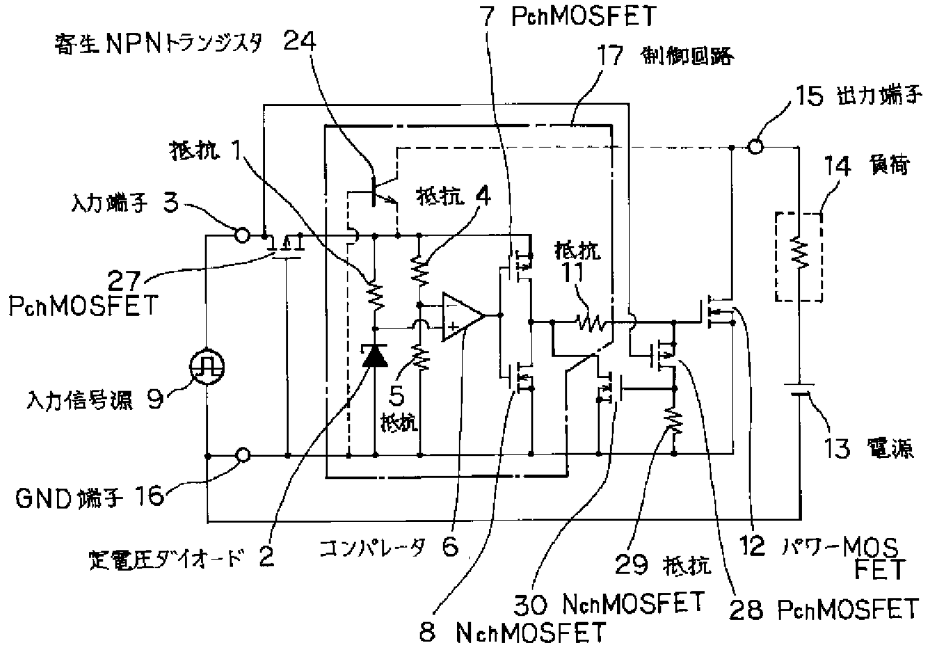
[Drawing 4]



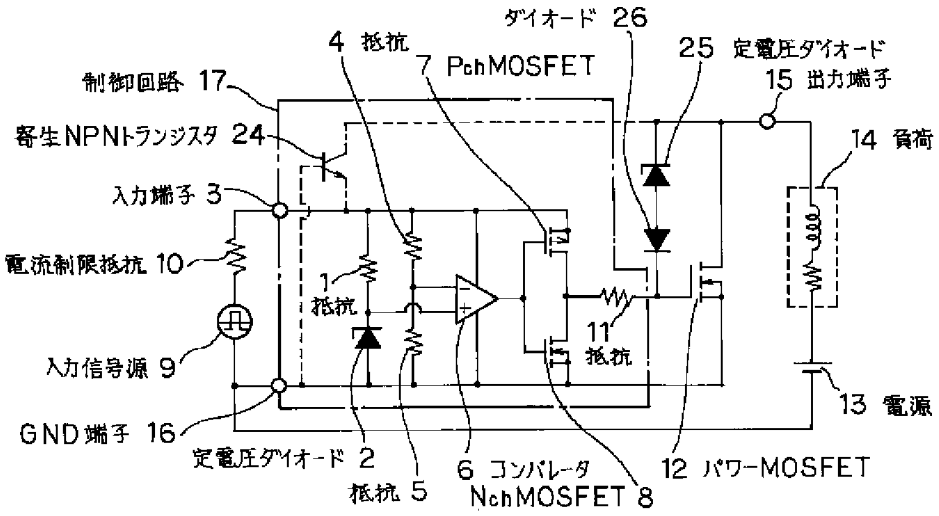
[Drawing 9]



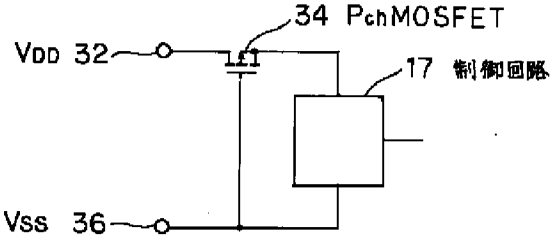
[Drawing 5]



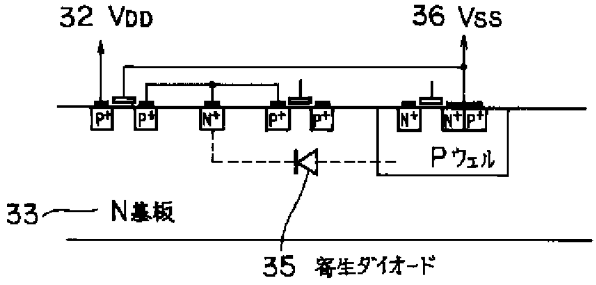
[Drawing 6]



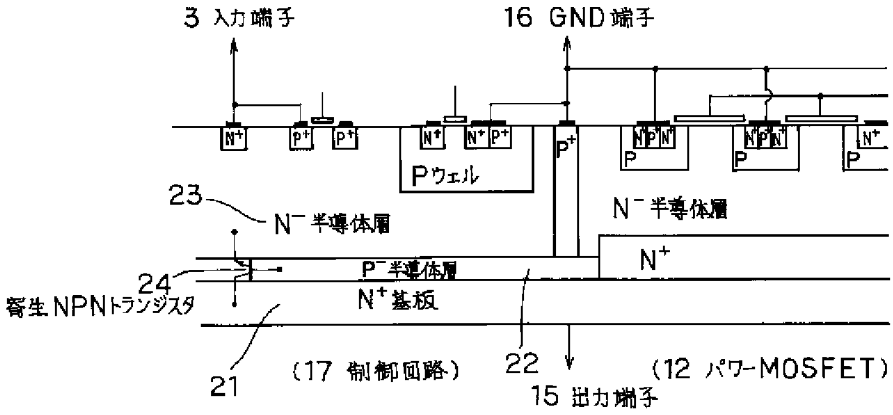
[Drawing 10]



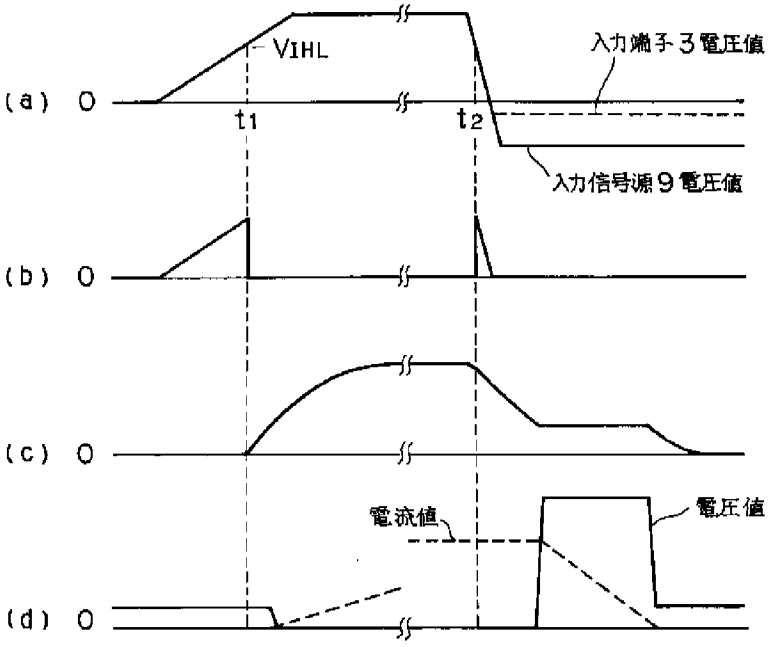
[Drawing 11]



[Drawing 7]



[Drawing 8]



[Translation done.]

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21/822			27/08	３２１Ｈ	
21/8238					
27/092					

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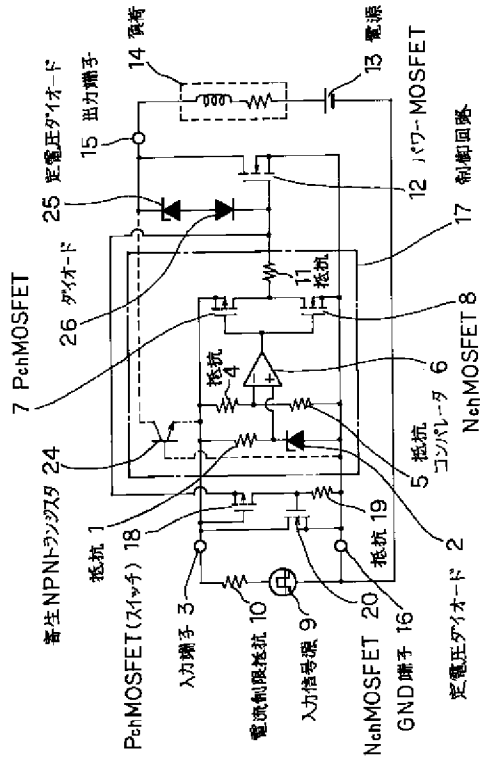
(54)【発明の名称】　半導体装置

(57)【要約】

【課題】　入力端子の電圧がＧＮＤ端子の電圧よりも低くなると、寄生ＮＰＮトランジスタが動作し、出力端子から入力端子に電流が流れて装置が破損してしまう。

【解決手段】　パワーＭＯＳＦＥＴに蓄積された電荷が放電される際、ＰchＭＯＳＦＥＴ１８の動作によりＮch ＭＯＳＦＥＴ２０がオン状態となり、それにより、寄生ＮＰＮトランジスタ２４のベース・エミッタ間が短絡され、寄生ＮＰＮトランジスタ２４の動作が回避される。



【特許請求の範囲】
【請求項１】　入力信号を発生させる入力信号源と、半導体基板を出力とし、負荷への電流の供給を制御するパワーＭＯＳＦＥＴと、
該パワーＭＯＳＦＥＴの動作を制御する制御回路と、
前記半導体基板と異なる導電型であり、前記半導体基板と接合された第１の半導体層に設けられたＧＮＤ端子と、
前記半導体基板と同じ導電型であり、前記第１の半導体層に接合された第２の半導体層に設けられた入力端子とを有し、
前記制御回路内に、エミッタ端子が前記第２の半導体層に接続され、コレクタ端子が前記半導体基板に接続され、ベース端子が前記第１の半導体層に接続された寄生トランジスタが存在する半導体装置において、
ドレイン端子が前記入力端子に接続され、ソース端子が前記ＧＮＤ端子に接続され、前記半導体基板と同型チャネルである第１のＭＯＳＦＥＴと、
前記入力端子における電圧値がローレベルの時に、前記パワーＭＯＳＦＥＴのゲート端子と前記第１のＭＯＳＦＥＴのゲート端子とを接続する第１のスイッチとを有することを特徴とする半導体装置。
【請求項２】　請求項１に記載の半導体装置において、
前記第１のスイッチは、前記第１のＭＯＳＦＥＴと異なる導電型のチャネルである第２のＭＯＳＦＥＴであることを特徴とする半導体装置。
【請求項３】　請求項１または請求項２に記載の半導体装置において、
前記制御回路に流れる電流を制御する電流制御回路を有することを特徴とする半導体装置。
【請求項４】　入力信号を発生させる入力信号源と、半導体基板を出力とし、負荷への電流の供給を制御するパワーＭＯＳＦＥＴと、
該パワーＭＯＳＦＥＴの動作を制御する制御回路と、
前記半導体基板と異なる導電型であり、前記半導体基板と接合された第１の半導体層に設けられたＧＮＤ端子と、
前記半導体基板と同じ導電型であり、前記第１の半導体層に接合された第２の半導体層に設けられた入力端子とを有し、
前記制御回路内に、エミッタ端子が前記第２の半導体層に接続され、コレクタ端子が前記半導体基板に接続され、ベース端子が前記第１の半導体層に接続された寄生トランジスタが存在する半導体装置において、
前記第２の半導体層と前記入力端子との間に、ドレイン端子が前記入力端子に接続され、ソース端子が前記第２の半導体層に接続され、ゲート端子が前記ＧＮＤ端子に接続された第３のＭＯＳＦＥＴを有することを特徴とする半導体装置。
【請求項５】　請求項４に記載の半導体装置において、
ドレイン端子が前記制御回路の出力段に接続され、ソース端子が前記ＧＮＤ端子に接続された第４のＭＯＳＦＥＴと、
前記入力端子における電圧値がローレベルの時に、前記パワーＭＯＳＦＥＴのゲート端子と前記第４のＭＯＳＦＥＴのゲート端子とを接続する第２のスイッチとを有することを特徴とする半導体装置。
【請求項６】　請求項５に記載の半導体装置において、
前記第２のスイッチは、前記半導体基板と異なる導電型のチャネルである第５のＭＯＳＦＥＴであることを特徴とする半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置に関し、特に、パワーＭＯＳＩＣに関する。
【０００２】
【従来の技術】図６は、従来の半導体装置の一構成例を示す回路図である。
【０００３】本従来例は図６に示すように、入力信号を発生させる入力信号源９と、装置に流れる電流を制限する電流制限抵抗１０と、電源１３と、負荷１４と、負荷１４への電流の供給を制御するパワーＭＯＳＦＥＴ１２と、定電圧ダイオード２５と、ダイオード２６と、パワーＭＯＳＦＥＴ１２の動作を制御する制御回路１７とから構成されており、制御回路１７には、入力端子３とＧＮＤ端子１６との間に並列に接続された抵抗１及び定電圧ダイオード２と、抵抗４，５と、抵抗４，５によって分圧された電圧値を比較するコンパレータ６と、コンパレータ６からの出力がゲート端子に入力されるPchＭＯＳＦＥＴ７及びNchＭＯＳＦＥＴ８と、一方がPchＭＯＳＦＥＴ７及びNchＭＯＳＦＥＴ８のドレイン端子に接続され、他方がパワーＭＯＳＦＥＴ１２のゲート端子に接続された抵抗１１とが設けられ、また、ベース端子がＧＮＤ端子１６に接続され、エミッタ端子が入力端子３に接続され、コレクタ端子が出力端子１５に接続された寄生ＮＰＮトランジスタ２４が存在している。
【０００４】図７は、図６に示した半導体装置の構造を示す断面図である。
【０００５】本従来例は図７に示すように、パワーＭＯＳＦＥＴ１２の出力となるN^+基板２１と、N^+基板２１上に接合されたP^-半導体層２２と、P^-半導体層２２上に接合され、制御回路１７を有しているN^-半導体層２３とから構成されている。
【０００６】以下に、上記のように構成された半導体装置の動作について説明する。
【０００７】図８は、図６及び図７に示した半導体装置の動作を説明するための図であり、（ａ）は入力信号源９から出力される信号の電圧及び入力端子３における電圧値を示す図、（ｂ）はコンパレータ６の出力電圧を示す図、（ｃ）はパワーＭＯＳＦＥＴ１２のゲート電圧を

示す図、（ｄ）は出力端子１５における電圧値及び電流値を示す図である。

【０００８】入力信号源９から出力される電圧が上昇し、抵抗４，５の分圧電圧値が定電圧ダイオード２の定電圧を越えると（ｔ１）、コンパレータ６の出力がローレベルとなる。

【０００９】すると、PchＭＯＳＦＥＴ７がオン状態となり、また、NchＭＯＳＦＥＴ８がオフ状態となる。

【００１０】これにより、パワーＭＯＳＦＥＴ１２のゲートに電荷が蓄積され、パワーＭＯＳＦＥＴ１２がオン状態となり、負荷１４に電流が流れる。

【００１１】次に、入力信号源９から出力される電圧が下がり、抵抗４，５の分圧電圧値が定電圧ダイオード２の定電圧以下になると（ｔ２）、コンパレータ６の出力がハイレベルとなる。

【００１２】すると、PchＭＯＳＦＥＴ７がオフ状態となり、また、NchＭＯＳＦＥＴ８がオン状態となる。

【００１３】これにより、パワーＭＯＳＦＥＴ１２のゲートに蓄積された電荷が放電され、パワーＭＯＳＦＥＴ１２がオフ状態に遷移していく。

【００１４】そして、負荷１４のリアクタンス成分により、出力端子１５の電圧が上昇し、出力端子１５の電圧が定電圧ダイオード２５の定電圧値を越えると、定電圧ダイオード２５、ダイオード２６及び抵抗１１を通り、NchＭＯＳＦＥＴ８からＧＮＤ端子１６あるいはPchＭＯＳＦＥＴ７のドレインから入力端子３に電流が流れる。

【００１５】これにより、パワーＭＯＳＦＥＴ１２のゲート電圧が引き続きバイアスされ、このバイアスによりパワーＭＯＳＦＥＴ１２に電流が流れるいわゆるダイナミッククランプ動作が行われる。

【００１６】

【発明が解決しようとする課題】しかしながら、上述したような従来の半導体装置においては、入力端子３の電圧がＧＮＤ端子１６の電圧よりも低くなると、寄生ＮＰＮトランジスタ２４が動作し、出力端子１５から入力端子３に電流が流れて装置が破損してしまうという問題点がある。

【００１７】すなわち、図７に示すように、上記従来例においては、寄生ＮＰＮトランジスタ２４が、N^+基板２１がコレクタ、P^-半導体層２２がベース、N^-半導体層２３がエミッタとなる構造であるため、出力端子１５に電圧が印加された状態で、入力端子３における電圧がＧＮＤ端子１６における電圧よりも低くなり、その差がベース・エミッタ間電圧を越えてＧＮＤ端子１６から入力端子３に電流が流れると、寄生ＮＰＮトランジスタ２４が動作してしまう。

【００１８】特に、ダイナミッククランプ動作時のように高い電圧（例えば７０Ｖ）が出力端子１５に印加されている場合には、バイポーラトランジスタ特有の二次降伏となり、装置の破損が発生しやすくなってしまう。

【００１９】そこで、特開平５－５８５８３号公報に半導体装置の破損を防ぐ装置が開示されている。

【００２０】図９は、特開平５－５８５８３号公報に開示された装置の概略を示すブロック図である。

【００２１】本装置は図９に示すように、入力端子３とＧＮＤ端子１６との間にスレッショルド電圧V_Iの高いＭＯＳＦＥＴ３１が接続されており、入力端子３に静電気が印加された場合に、入力端子３とＧＮＤ端子１６との間の電圧がスレッショルド電圧V_I（本例では２０～２５Ｖ程度）を越えると、二次ブレークダウンによりＭＯＳＦＥＴ３１を導通させるものである。

【００２２】しかしながら、図６に示した半導体装置における問題点は、入力端子３の電圧がＧＮＤ端子１６の電圧より低い時に寄生ＮＰＮトランジスタ２４が動作することにより発生する装置の破損であるため、図９に示した公知例は意味をなさない。

【００２３】また、他の公知例として、「Reverse-Voltage Protection Methods for CMOSCircuits」（IEEE JOURNAL Vol24,Feb.1989）のSupply Terminal Protectionがある。

【００２４】図１０は、「Reverse-Voltage Protection Methods for CMOS Circuits」（IEEE JOURNAL Vol24,Feb.1989）に開示された装置の概略を示すブロック図であり、図１１は、図１０に示した装置の構造を示す断面図である。

【００２５】本装置は図１０及び図１１に示すように、V_{DD}３２とＮ基板３３との間にPchＭＯＳＦＥＴ３４を接続したもので、$V_{DD}＜V_{SS}$時に寄生ダイオード３５を介して短絡電流が流れることを防ぐものである。

【００２６】しかしながら、図６に示した半導体装置においては、電流制限抵抗１０が挿入されているため、V_{DD}３２を入力、V_{SS}をＧＮＤと置き換えても短絡電流を防ぐ対策は不要である。また、図１０及び図１１に示した装置に、パワーＭＯＳＦＥＴを搭載すると、高耐圧横型のパワーＭＯＳＦＥＴになるため、オン抵抗が大きくなり（例えば７０Ｖ耐圧で１．５倍程度）不適当である。

【００２７】本発明は、上述したような従来の技術が有する問題点に鑑みてなされたものであって、寄生トランジスタが動作することにより発生する装置の破損を防ぐことができる半導体装置を提供することを目的とする。

【００２８】

【課題を解決するための手段】上記目的を達成するために本発明は、入力信号を発生させる入力信号源と、半導体基板を出力とし、負荷への電流の供給を制御するパワーＭＯＳＦＥＴと、該パワーＭＯＳＦＥＴの動作を制御する制御回路と、前記半導体基板と異なる導電型であり、前記半導体基板と接合された第１の半導体層に設けられたＧＮＤ端子と、前記半導体基板と同じ導電型であ

り、前記第１の半導体層に接合された第２の半導体層に設けられた入力端子とを有し、前記制御回路内に、エミッタ端子が前記第２の半導体層に接続され、コレクタ端子が前記半導体基板に接続され、ベース端子が前記第１の半導体層に接続された寄生トランジスタが存在する半導体装置において、ドレイン端子が前記入力端子に接続され、ソース端子が前記ＧＮＤ端子に接続され、前記半導体基板と同型チャネルである第１のＭＯＳＦＥＴと、前記入力端子における電圧値がローレベルの時に、前記パワーＭＯＳＦＥＴのゲート端子と前記第１のＭＯＳＦＥＴのゲート端子とを接続する第１のスイッチとを有することを特徴とする。

【００２９】また、前記第１のスイッチは、前記第１のＭＯＳＦＥＴと異なる導電型のチャネルである第２のＭＯＳＦＥＴであることを特徴とする。

【００３０】また、前記制御回路に流れる電流を制御する電流制御回路を有することを特徴とする。

【００３１】また、入力信号を発生させる入力信号源と、半導体基板を出力とし、負荷への電流の供給を制御するパワーＭＯＳＦＥＴと、該パワーＭＯＳＦＥＴの動作を制御する制御回路と、前記半導体基板と異なる導電型であり、前記半導体基板と接合された第１の半導体層に設けられたＧＮＤ端子と、前記半導体基板と同じ導電型であり、前記第１の半導体層に接合された第２の半導体層に設けられた入力端子とを有し、前記制御回路内に、エミッタ端子が前記第２の半導体層に接続され、コレクタ端子が前記半導体基板に接続され、ベース端子が前記第１の半導体層に接続された寄生トランジスタが存在する半導体装置において、前記第２の半導体層と前記入力端子との間に、ドレイン端子が前記入力端子に接続され、ソース端子が前記第２の半導体層に接続され、ゲート端子が前記ＧＮＤ端子に接続された第３のＭＯＳＦＥＴを有することを特徴とする。

【００３２】また、ドレイン端子が前記制御回路の出力段に接続され、ソース端子が前記ＧＮＤ端子に接続された第４のＭＯＳＦＥＴと、前記入力端子における電圧値がローレベルの時に、前記パワーＭＯＳＦＥＴのゲート端子と前記第４のＭＯＳＦＥＴのゲート端子とを接続する第２のスイッチとを有することを特徴とする。

【００３３】また、前記第２のスイッチは、前記半導体基板と異なる導電型のチャネルである第５のＭＯＳＦＥＴであることを特徴とする。

【００３４】（作用）上記のように構成された本発明においては、パワーＭＯＳＦＥＴに蓄積された電荷が放電される際、第１のスイッチの動作により第１のＭＯＳＦＥＴがオン状態となり、それにより、寄生トランジスタのベース・エミッタ間が短絡されるので、寄生トランジスタが動作することはない。

【００３５】また、第３のＭＯＳＦＥＴのソース電圧が下がってゲート電圧との差がスレッショルド電圧となったときに第３のＭＯＳＦＥＴがオフ状態となるので、寄生トランジスタのエミッタ電圧がベース電圧よりも低くなることはなく、寄生トランジスタが動作することはない。

【００３６】

【発明の実施の形態】以下に、本発明の実施の形態について図面を参照して説明する。

【００３７】（第１の実施の形態）図１は、本発明の半導体装置の第１の実施の形態を示す回路図であり、図２は、図１に示した半導体装置の構造を示す断面図である。

【００３８】本形態は図１に示すように、入力信号を発生させる入力信号源９と、装置に流れる電流を制限する電流制限抵抗１０と、電源１３と、負荷１４と、負荷１４への電流の供給を制御するパワーＭＯＳＦＥＴ１２と、定電圧ダイオード２５と、ダイオード２６と、パワーＭＯＳＦＥＴ１２の動作を制御する制御回路１７と、制御回路１７の入力端子３とＧＮＤ端子１６間に並列に接続された第１のＭＯＳＦＥＴであるＮchＭＯＳＦＥＴ２０と、ＮchＭＯＳＦＥＴ２０の動作を制御する第１のスイッチとなる第２のＭＯＳＦＥＴであるＰchＭＯＳＦＥＴ１８と、ＰchＭＯＳＦＥＴ１８と直列に接続された抵抗１９とから構成されており、制御回路１７には、入力端子３とＧＮＤ端子１６との間に並列に接続された抵抗１及び定電圧ダイオード２と、抵抗４，５と、抵抗４，５によって分圧された電圧値を比較するコンパレータ６と、コンパレータ６からの出力がゲート端子に入力されるＰchＭＯＳＦＥＴ７及びＮchＭＯＳＦＥＴ８と、一方がＰchＭＯＳＦＥＴ７及びＮchＭＯＳＦＥＴ８のドレイン端子に接続され、他方がパワーＭＯＳＦＥＴ１２のゲート端子に接続された抵抗１１とが設けられ、また、ベース端子がＧＮＤ端子１６に接続され、エミッタ端子が入力端子３に接続され、コレクタ端子が出力端子１５に接続された寄生ＮＰＮトランジスタ２４が存在している。なお、ＮchＭＯＳＦＥＴ２０においては、ゲート端子が抵抗１９を介してＧＮＤ端子１６に接続され、ソース端子がＧＮＤ端子１６に接続され、ドレイン端子が入力端子３に接続されており、ＰchＭＯＳＦＥＴ１８においては、ゲート端子が入力端子３に接続され、ドレイン端子がＮchＭＯＳＦＥＴ２０のゲート端子に接続され、ソース端子がパワーＭＯＳＦＥＴ１２のゲート端子に接続されている。

【００３９】上記のように構成された半導体装置においては、抵抗１と定電圧ダイオード２とによって基準電圧が生成され、この基準電圧と入力端子３から入力されて抵抗４，５で分圧された電圧値とがコンパレータ６において比較されている。

【００４０】また、本形態は図２に示すように、パワーＭＯＳＦＥＴ１２の出力となるN^+基板２１と、N^+基板２１上に接合された第１の半導体層であるP^-半導体層

２２と、P^-半導体層２２上に接合され、制御回路１７を有している第２の半導体層であるN^-半導体層２３とから構成されており、出力端子１５はN^+基板２１上に、入力端子３はN^-半導体層２３上に、ＧＮＤ端子１６はP^-半導体層２２上にそれぞれ設けられている。

【００４１】以下に、上記のように構成された半導体装置の動作について説明する。

【００４２】入力信号源９から出力される電圧が上昇し、抵抗４，５の分圧電圧値が定電圧ダイオード２の定電圧を越えると、コンパレータ６の出力がローレベルとなる。

【００４３】すると、ＰchＭＯＳＦＥＴ７がオン状態となり、また、ＮchＭＯＳＦＥＴ８がオフ状態となる。

【００４４】これにより、パワーＭＯＳＦＥＴ１２のゲートに電荷が蓄積され、パワーＭＯＳＦＥＴ１２がオン状態となり、電源１３から負荷１４、出力端子１５及びＧＮＤ端子１６に電流が流れる。

【００４５】次に、入力信号源９から出力される電圧が下がり、抵抗４，５の分圧電圧値が定電圧ダイオード２の定電圧以下になると、コンパレータ６の出力がハイレベルとなる。

【００４６】すると、ＰchＭＯＳＦＥＴ７がオフ状態となり、また、ＮchＭＯＳＦＥＴ８がオン状態となる。

【００４７】これにより、パワーＭＯＳＦＥＴ１２のゲートに蓄積された電荷が放電され始めるが、この際、ＰchＭＯＳＦＥＴ１８がオン状態となり、それにより、抵抗１９に電圧が印加されてＮchＭＯＳＦＥＴ２０がオン状態となる。

【００４８】これにより、図２に示すように、パワーＭＯＳＦＥＴ１２の出力となるN^+基板２１をコレクタとし、ＧＮＤ端子１６に接続されているP^-半導体層２２をベースとし、入力端子３に接続されているN^-半導体層２３をエミッタとする寄生ＮＰＮトランジスタ２４のベース・エミッタ間が短絡されることとなり、入力信号源９における電圧がＧＮＤ端子１６における電圧以下の場合でも、ベース・エミッタ間の電圧差を寄生ＮＰＮトランジスタ２４のベース・エミッタ間動作電圧（約０．７Ｖ）よりも小さくすることができるため、寄生ＮＰＮトランジスタ２４の動作が回避される。

【００４９】次に、パワーＭＯＳＦＥＴ１２のゲート電圧が下がると、出力端子１５における電圧が上昇し、定電圧ダイオード２５、ダイオード２６、抵抗１１及びＰchＭＯＳＦＥＴ７のドレイン・ソース間を通って、入力端子３あるいはＰchＭＯＳＦＥＴ１８、抵抗１９及びＧＮＤ端子１６に電流が流れる。

【００５０】この電流によりパワーＭＯＳＦＥＴ１２のゲートがバイアスされるため、負荷１４のリアクタンスに蓄積されていたエネルギーが放出され、出力端子１５における電圧が下がるまで、ＰchＭＯＳＦＥＴ１８がオン状態、すなわちＮchＭＯＳＦＥＴ２０がオン状態となり、出力端子１５における電圧が高い時に寄生ＮＰＮトランジスタ２４が動作することを防ぐことができる。

【００５１】（第２の実施の形態）図３は、本発明の半導体装置の第２の実施の形態を示す回路図である。

【００５２】本形態は図３に示すように、入力信号を発生させる入力信号源９と、電源１３と、負荷１４と、負荷１４への電流の供給を制御するパワーＭＯＳＦＥＴ１２と、パワーＭＯＳＦＥＴ１２の動作を制御する制御回路１７と、入力信号源９と制御回路１７との間に接続された第３のＭＯＳＦＥＴであるＰchＭＯＳＦＥＴ２７とから構成されており、制御回路１７には、ＰchＭＯＳＦＥＴ２７のソース端子とＧＮＤ端子１６との間に並列に接続された抵抗１及び定電圧ダイオード２と、抵抗４，５と、抵抗４，５によって分圧された電圧値を比較するコンパレータ６と、コンパレータ６からの出力がゲート端子に入力されるＰchＭＯＳＦＥＴ７及びＮchＭＯＳＦＥＴ８と、一方がＰchＭＯＳＦＥＴ７及びＮchＭＯＳＦＥＴ８のドレイン端子に接続され、他方がパワーＭＯＳＦＥＴ１２のゲート端子に接続された抵抗１１とが設けられ、また、ベース端子がＧＮＤ端子１６に接続され、エミッタ端子がＰchＭＯＳＦＥＴ２７のソース端子に接続され、コレクタ端子が出力端子１５に接続された寄生ＮＰＮトランジスタ２４が存在している。なお、ＰchＭＯＳＦＥＴ２７においては、ゲート端子がＧＮＤ端子１６に接続され、ソース端子が制御回路１７に接続され、ドレイン端子が入力端子３に接続されている。

【００５３】以下に、上記のように構成された半導体装置の動作について説明する。

【００５４】入力信号源９における電圧が上昇し、ＰchＭＯＳＦＥＴ２７のドレイン・ソース間ダイオード電圧（約０．７Ｖ）とスレッショルド電圧（約１Ｖ）との和を越えると、ＰchＭＯＳＦＥＴ２７がオン状態となり、さらに入力信号源９における電圧が上昇し、ハイレベルとなると制御回路１７の動作により、パワーＭＯＳＦＥＴ１２のゲートに電荷が蓄積され、パワーＭＯＳＦＥＴ１２がオン状態となる。

【００５５】次に、入力信号源９の電圧が下がり、ＧＮＤ端子１６における電圧以下になると、パワーＭＯＳＦＥＴ１２のゲートに蓄積された電荷が、抵抗１１及びＰchＭＯＳＦＥＴ７のドレイン・ソース間ダイオードを経て、ゲートがバイアスされているＰchＭＯＳＦＥＴ２７から入力端子３に流れ出す。

【００５６】図４は、図３に示した半導体装置の動作を説明するための図であり、（ａ）は入力端子３における電圧値を示す図、（ｂ）はＰchＭＯＳＦＥＴ２７のソース電圧を示す図、（ｃ）は出力端子１５における電圧値及び電流値を示す図である。

【００５７】ＰchＭＯＳＦＥＴ２７のソース電圧が、制御回路１７のローレベル・ハイレベルの判定電圧V_{IHL}に達すると、ＮchＭＯＳＦＥＴ８がオン状態となり、こ

れにより、PchＭＯＳＦＥＴ２７のソース電圧がほぼ零電圧となり、制御回路１７が動作しなくなる。

【００５８】したがって、NchＭＯＳＦＥＴ８がオフ状態という不安定な状態においてパワーＭＯＳＦＥＴ１２のゲートに蓄積された電荷が放電し、放電が完了すると、パワーＭＯＳＦＥＴ１２はオフ状態となる。

【００５９】この時、PchＭＯＳＦＥＴ２７のソース電圧は、徐々に下がってくるが、スレッショルド電圧（約１Ｖ）にてPchＭＯＳＦＥＴ２７がオフ状態となるため、ＧＮＤ端子１６における電圧以下にはならない。したがって、寄生ＮＰＮトランジスタ２４が動作することはない。

【００６０】以上説明したように本形態においては、入力信号源９における電圧がＧＮＤ端子１６における電圧以下になると、パワーＭＯＳＦＥＴ１２のゲートに蓄積された電荷が放電し、放電が完了するまでPchＭＯＳＦＥＴ２７に電流が流れ、放電が完了すると、電流が流れないという動作となるため、寄生トランジスタが動作することはない。

【００６１】（第３の実施の形態）図５は、本発明の半導体装置の第３の実施の形態を示す回路図である。

【００６２】本形態は図５に示すように、入力信号を発生させる入力信号源９と、電源１３と、負荷１４と、負荷１４への電流の供給を制御するパワーＭＯＳＦＥＴ１２と、パワーＭＯＳＦＥＴ１２の動作を制御する制御回路１７と、制御回路１７の出力段に接続された第４のＭＯＳＦＥＴであるNchＭＯＳＦＥＴ３０と、NchＭＯＳＦＥＴ３０の動作を制御する第２のスイッチとなる第５のＭＯＳＦＥＴであるPchＭＯＳＦＥＴ２８と、PchＭＯＳＦＥＴ２８と直列に接続された抵抗２９と、入力信号源９と制御回路１７との間に接続されたPchＭＯＳＦＥＴ２７とから構成されており、制御回路１７には、PchＭＯＳＦＥＴ２７のソース端子とＧＮＤ端子１６との間に並列に接続された抵抗１及び定電圧ダイオード２と、抵抗４，５と、抵抗４，５によって分圧された電圧値を比較するコンパレータ６と、コンパレータ６からの出力がゲート端子に入力されるPchＭＯＳＦＥＴ７及びNchＭＯＳＦＥＴ８と、一方がPchＭＯＳＦＥＴ７及びNchＭＯＳＦＥＴ８のドレイン端子に接続され、他方がパワーＭＯＳＦＥＴ１２のゲート端子に接続された抵抗１１とが設けられ、また、ベース端子がＧＮＤ端子１６に接続され、エミッタ端子がPchＭＯＳＦＥＴ２７のソース端子に接続され、コレクタ端子が出力端子１５に接続された寄生ＮＰＮトランジスタ２４が存在している。なお、NchＭＯＳＦＥＴ３０においては、ゲート端子が抵抗２９を介してＧＮＤ端子１６に接続され、ソース端子がＧＮＤ端子１６に接続され、ドレイン端子がPchＭＯＳＦＥＴ７及びNchＭＯＳＦＥＴ８のドレイン端子に接続されており、PchＭＯＳＦＥＴ２８においては、ゲート端子が入力端子３に接続され、ドレイン端子がNchＭＯＳＦＥＴ３０のゲート端子に接続され、ソース端子がパワーＭＯＳＦＥＴ１２のゲート端子に接続されている。

【００６３】以下に、上記のように構成された半導体装置の動作について説明する。

【００６４】入力信号源９における電圧がＧＮＤ端子１６における電圧以下になると、PchＭＯＳＦＥＴ２８がオン状態となり、それにより、NchＭＯＳＦＥＴ３０がオン状態となる。

【００６５】そして、パワーＭＯＳＦＥＴ１２のゲートに蓄積された電荷は、抵抗１１、NchＭＯＳＦＥＴ３０を通って放電する。

【００６６】したがって、制御回路１７は不安定な動作とはならず、オフ状態になるとともに、PchＭＯＳＦＥＴ２７のゲート・ソース間電圧がほぼ零となるため、PchＭＯＳＦＥＴ２７には電流が流れなくなる。

【００６７】そのため、入力信号源９から出力される信号が、ドライブ能力の少ない他の半導体装置等による場合でも、高速のターンオフ時間を確保することができる。

【００６８】なお、上述した実施の形態においては、NchパワーＭＯＳＦＥＴを用いて寄生ＮＰＮトランジスタが存在する回路について説明したが、PchＭＯＳＦＥＴを用いて寄生ＰＮＰトランジスタが存在する場合には、PchＭＯＳＦＥＴ１８をNchＭＯＳＦＥＴ、NchＭＯＳＦＥＴ２０をPchＭＯＳＦＥＴ、PchＭＯＳＦＥＴ２７をNchＭＯＳＦＥＴ、PchＭＯＳＦＥＴ２８をNchＭＯＳＦＥＴ、NchＭＯＳＦＥＴ３０をPchＭＯＳＦＥＴとすることにより、同様の効果を上げることができる。

【００６９】

【発明の効果】本発明は、以上説明したように構成されているので、以下に記載するような効果を奏する。

【００７０】請求項１から３に記載のものにおいては、パワーＭＯＳＦＥＴに蓄積された電荷が放電される際に、第１のスイッチの動作により第１のＭＯＳＦＥＴがオン状態となり、それにより、寄生トランジスタのベース・エミッタ間が短絡される構成としたため、寄生トランジスタが動作することはなく、半導体装置の破損を防ぐことができる。

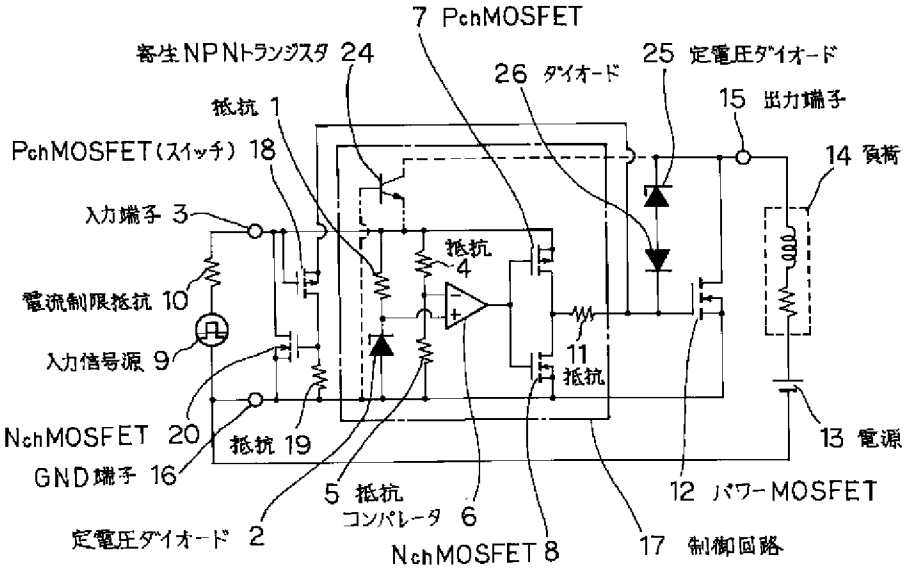
【００７１】請求項４及び５に記載のものにおいては、第３のＭＯＳＦＥＴのソース電圧が下がってゲート電圧との差がスレッショルド電圧となったときに第３のＭＯＳＦＥＴがオフ状態となる構成としたため、寄生トランジスタのエミッタ電圧がベース電圧よりも低くなることはなく、寄生トランジスタが動作することはない。それにより、寄生トランジスタの動作により発生する半導体装置の破損を防ぐことができる。

【図面の簡単な説明】

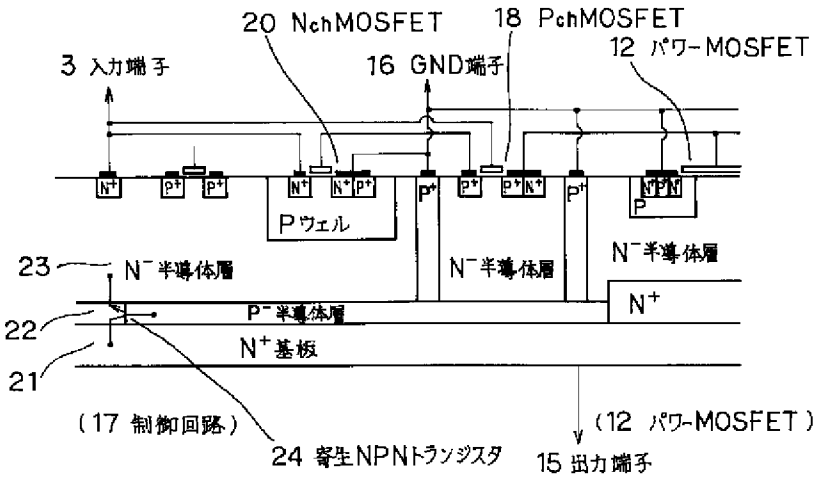
【図１】本発明の半導体装置の第１の実施の形態を示す回路図である。

【図２】図１に示した半導体装置の構造を示す断面図である。
【図３】本発明の半導体装置の第２の実施の形態を示す回路図である。
【図４】図３に示した半導体装置の動作を説明するための図であり、（ａ）は入力端子における電圧値を示す図、（ｂ）はＰｃｈＭＯＳＦＥＴのソース電圧を示す図、（ｃ）は出力端子における電圧値及び電流値を示す図である。
【図５】本発明の半導体装置の第３の実施の形態を示す回路図である。
【図６】従来の半導体装置の一構成例を示す回路図である。
【図７】図６に示した半導体装置の構造を示す断面図である。
【図８】図６及び図７に示した半導体装置の動作を説明するための図であり、（ａ）は入力信号源９から出力される信号の電圧及び入力端子３における電圧値を示す図、（ｂ）はコンパレータ６の出力電圧を示す図、（ｃ）はパワーＭＯＳＦＥＴ１２のゲート電圧を示す図、（ｄ）は出力端子１５における電圧値及び電流値を示す図である。
【図９】特開平５－５８５８３号公報に開示された装置の概略を示すブロック図である。
【図１０】「Reverse-Voltage Protection Methods for CMOS Circuits」（IEEE JOURNALVol24,Feb.1989）に開示された装置の概略を示すブロック図である。
【図１１】図１０に示した装置の構造を示す断面図である。
【符号の説明】
１，４，５，１１，１９，２９　　抵抗
２，２５　　定電圧ダイオード
３　　入力端子
６　　コンパレータ
７，１８，２７，２８，３４　　ＰｃｈＭＯＳＦＥＴ
８，２０，３０　　ＮｃｈＭＯＳＦＥＴ
９　　入力信号源
１０　　電流制限抵抗
１２　　パワーＭＯＳＦＥＴ
１３　　電源
１４　　負荷
１５　　出力端子
１６　　ＧＮＤ端子
１７　　制御回路
２１　　N^+基板
２２　　P^-半導体層
２３　　N^-半導体層
２４　　寄生ＮＰＮトランジスタ
２６　　ダイオード

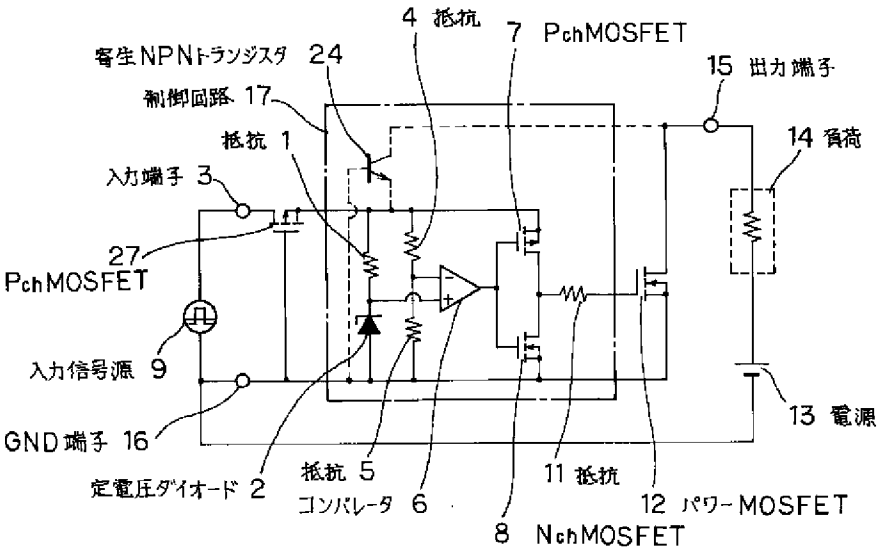
【図１】



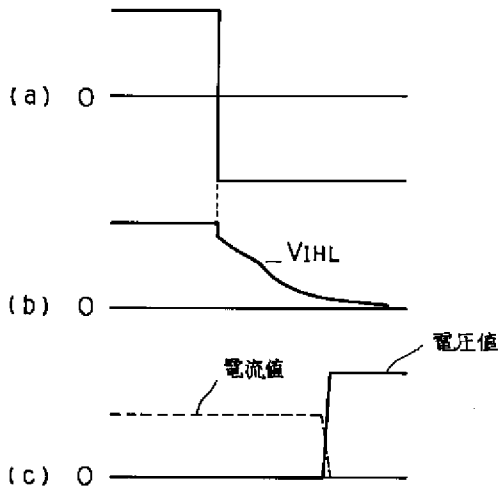
【図2】


20 NchMOSFET
18 PchMOSFET
12 パワーMOSFET
3 入力端子
16 GND端子
Pウェル
23
N⁻半導体層
22
P⁻半導体層
N⁺
21
N⁺基板
（17 制御回路）
24 寄生NPNトランジスタ
15 出力端子
（12 パワーMOSFET）

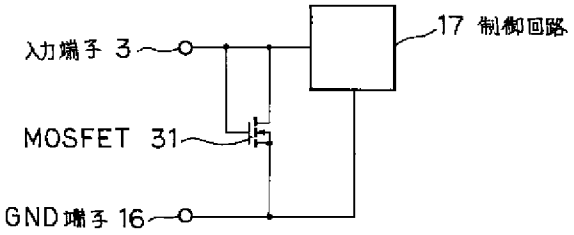
【図3】


4 抵抗
7 PchMOSFET
寄生NPNトランジスタ 24
15 出力端子
制御回路 17
抵抗 1
14 負荷
入力端子 3
27
PchMOSFET
入力信号源 9
GND端子 16
13 電源
定電圧ダイオード 2
抵抗 5
コンパレータ 6
11 抵抗
12 パワーMOSFET
8 NchMOSFET

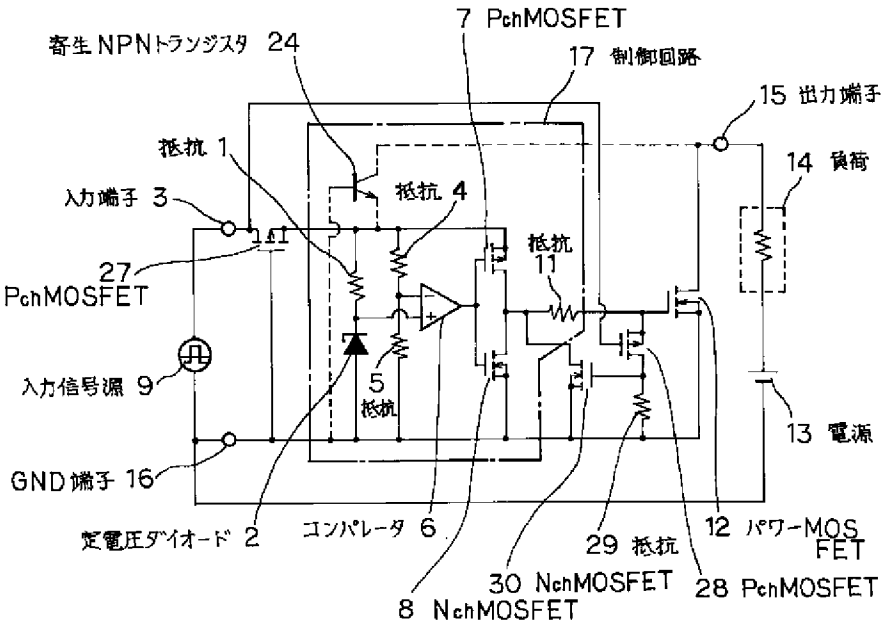
【図4】


(a) 0
VIHL
(b) 0
電流値
電圧値
(c) 0

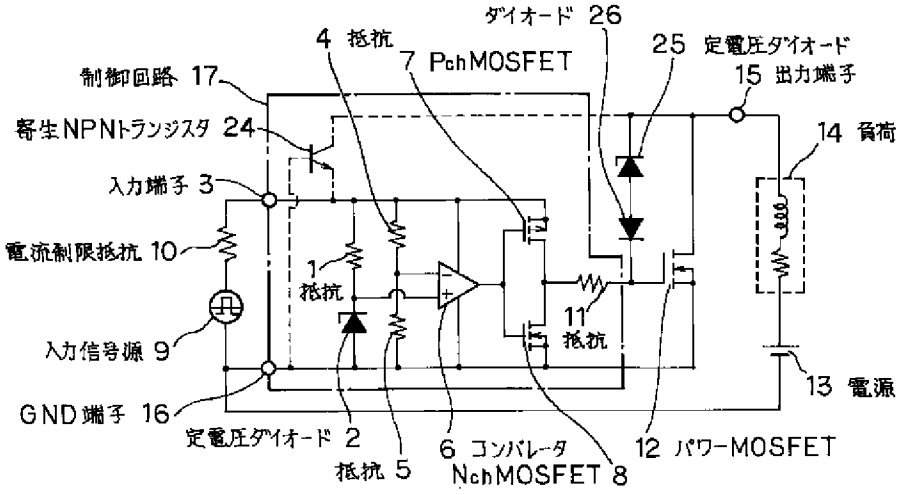
【図9】


17 制御回路
入力端子 3
MOSFET 31
GND端子 16

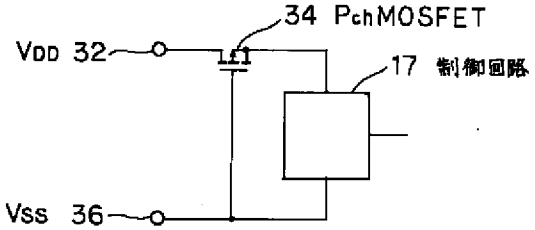
【図5】


寄生NPNトランジスタ 24
7 PchMOSFET
17 制御回路
15 出力端子
抵抗 1
抵抗 4
14 負荷
入力端子 3
抵抗
11
27
PchMOSFET
入力信号源 9
5
抵抗
13 電源
GND端子 16
定電圧ダイオード 2
コンパレータ 6
29 抵抗
12 パワーMOS
FET
30 NchMOSFET
28 PchMOSFET
8 NchMOSFET

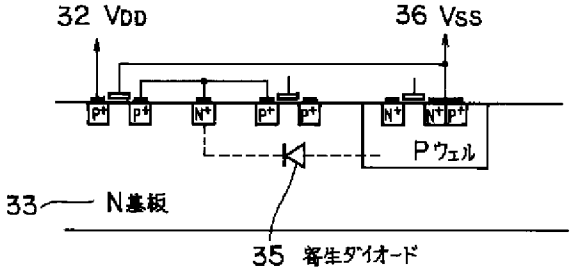
【図6】


ダイオード 26
4 抵抗
25 定電圧ダイオード
7 PchMOSFET
15 出力端子
制御回路 17
寄生NPNトランジスタ 24
14 負荷
入力端子 3
電流制限抵抗 10
1
抵抗
11
抵抗
入力信号源 9
13 電源
GND端子 16
定電圧ダイオード 2
抵抗 5
6 コンパレータ
NchMOSFET 8
12 パワーMOSFET

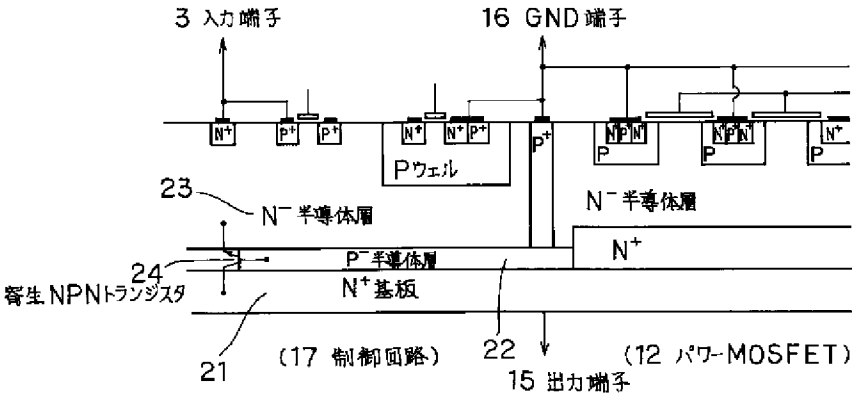
【図10】


34 PchMOSFET
VDD 32
17 制御回路
Vss 36

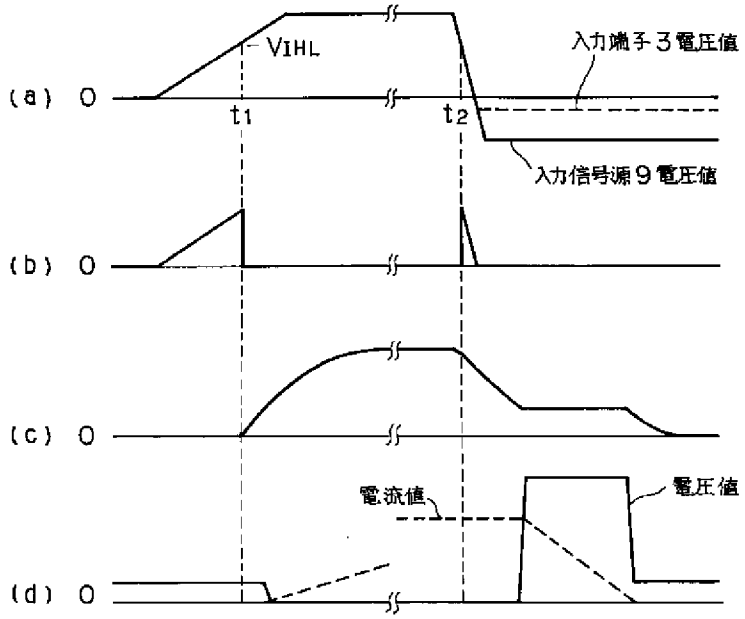
【図11】


32 VDD
36 Vss
P+
N+
Pウェル
33 N基板
35 寄生ダイオード

【図7】


3 入力端子
16 GND端子
N+
P+
Pウェル
P
N
23
N⁻半導体層
24
寄生NPNトランジスタ
P⁻半導体層
N+基板
N+
21
(17 制御回路)
22
15 出力端子
(12 パワーMOSFET)

【図8】


(a)
(b)
(c)
(d)
O
VIHL
t1
t2
入力端子3電圧値
入力信号源9電圧値
電流値
電圧値